

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

ACQIS LLC,

Plaintiff,

v.

MICROSOFT CORPORATION,

Defendant.

Case No. 6:22-cv-385-ADA

**JURY TRIAL DEMANDED**

ACQIS LLC,

Plaintiff,

v.

SONY INTERACTIVE ENTERTAINMENT  
INC., SONY INTERACTIVE  
ENTERTAINMENT LLC,

Defendants.

Case No. 6:22-cv-386-ADA

**JURY TRIAL DEMANDED**

**PLAINTIFF ACQIS LLC'S CONSOLIDATED RESPONSIVE**  
**CLAIM CONSTRUCTION BRIEF**

## TABLE OF CONTENTS

	Page
I. INTRODUCTION .....	1
II. THE ACQIS INVENTIONS.....	1
III. ISSUE PRECLUSION DOES NOT AFFECT THE ASSERTED CLAIMS .....	2
A. The Claim Scope Issues Here Are Not Identical to the Issues in <i>EMC</i> .....	3
B. The Issues of Claim Scope Here Were Not Actually Litigated or Necessary to the Judgment in <i>EMC</i> .....	7
IV. CLAIM CONSTRUCTION.....	9
A. “low voltage differential signal (LVDS) [channel]” / “LVDS [channel]” .....	9
B. “Peripheral Component Interconnect (PCI) bus transaction” / “PCI bus transaction” .....	14
1. “Backwards Compatible” Does Not Conflict with the Federal Circuit’s Decision in <i>EMC</i> .....	15
2. The Intrinsic Record Supports “Backwards Compatible.” .....	16
3. ACQIS’s Proposed Construction Is Consistent with ACQIS’s Previous Statements to the PTAB and <i>EMC</i> District Court. ....	17
C. “convey [/conveying/conveys/communicating/communicate/transmitting] ... a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]” .....	18
1. IPR Disclaimer Does Not Apply to the Asserted Claims. ....	19
2. The Specifications of the Asserted Patents Do Not Show Control Bits Being Part of a PCI Bus Transaction.....	22
D. “of a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]” .....	22
E. Claims reciting a [Peripheral Component Interconnect] PCI bus transaction, or an encoded [Peripheral Component Interconnect] PCI bus transaction, “in [a] serial form” or “serially encoded” or “in a serial bit stream” .....	24
F. “console”.....	27
G. “USB” / “Universal Serial Bus (USB) protocol” / “Universal Serial Bus (USB) protocol [data/information]” .....	28

H.	“serial bit channels” and “serial channel” .....	30
----	--	----

## TABLE OF AUTHORITIES

	Page
<b>Cases</b>	
<i>Abtox, Inc. v. Exitron Corp.</i> , 131 F.3d 1009 (Fed. Cir. 1997) .....	6
<i>ACQIS LLC v. Alcatel-Lucent USA Inc.</i> , No. 6:13-cv-638, 2015 WL 1737853 (E.D. Tex. Apr. 13, 2015) .....	27
<i>ACQIS LLC v. ASUSTeK Computer Inc.</i> , No. 6:20-cv-966-ADA, Dkt. 52 (W.D. Tex. Nov. 17, 2021).....	5, 17, 27, 28
<i>ACQIS LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:20-cv-295-JRG, Dkt. 92 (E.D. Tex. Sept. 26, 2021) .....	3, 5, 15, 20, 26
<i>ACQIS, LLC v. Appro Int’l, Inc.</i> , No. 6:09-cv-148, 2011 WL 382556 (E.D. Tex. Feb. 3, 2011).....	17
<i>ACQIS, LLC v. EMC Corp.</i> , No. 14-cv-13560, 2017 WL 6211051 (D. Mass. Dec. 8, 2017) .....	3, 4, 5, 6, 7, 15, 17, 25, 26
<i>ACQIS, LLC v. EMC Corp.</i> , No. 14-cv-13560, 2021 WL 1088207 (D. Mass. Feb. 19, 2021).....	2, 4, 5, 6, 7, 8, 25
<i>ACQIS, LLC v. EMC Corp.</i> , No. 2021-1772, 2022 WL 1562847 (Fed. Cir. May 18, 2022).....	2, 3, 5, 6, 8, 15
<i>Allergan Sales, LLC v. Sandoz Inc.</i> , No. 2:12-cv-207-JRG, 2016 WL 1224868, (E.D. Tex. Mar. 29, 2016) .....	7
<i>Avid Tech., Inc. v. Harmonic, Inc.</i> , 812 F.3d 1040 (Fed. Cir. 2016) .....	22
<i>Cox Commc’ns, Inc. v. Sprint Commc’n Co. LP</i> , 838 F.3d 1224 (Fed. Cir. 2016) .....	14
<i>Eibel Process Co. v. Minn. &amp; Ontario Paper Co.</i> , 261 U.S. 45 (1923).....	13
<i>Eko Brands, LLC v. Adrian Rivera Maynez Enters., Inc.</i> , 946 F.3d 1367 (Fed. Cir. 2020) .....	19
<i>Fenner Invs., Ltd. v. Cellco P’ship</i> , 778 F.3d 1320 (Fed. Cir. 2015) .....	4

<i>Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:17-cv-145-JRG-RSP, 2018 WL 647734 (E.D. Tex. Jan. 31, 2018) .....	29
<i>In re Rambus Inc.</i> , 694 F.3d 42 (Fed. Cir. 2012) .....	6
<i>Nautilus, Inc. v. Biosig Instruments, Inc.</i> , 572 U.S. 898 (2014).....	13
<i>Ohio Willow Wood Co. v. Alps South, LLC</i> , 735 F.3d 1333 (Fed. Cir. 2013) .....	7
<i>One-E-Way, Inc. v. Int’l Trade Comm’n</i> , 859 F.3d 1059 (Fed. Cir. 2017) .....	13
<i>Pfizer, Inc. v. Teva Pharms. USA, Inc.</i> , 429 F.3d 1364 (Fed. Cir. 2005) .....	7, 19
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) .....	2, 7, 8
<i>SightSound Techs., LLC v. Apple Inc.</i> , 809 F.3d 1307 (Fed. Cir. 2015) .....	6
<i>State Farm Mut. Auto. Ins. Co. v. LogistiCare Sols., LLC</i> , 751 F.3d 684 (5th Cir. 2014) .....	3, 5
<i>TecSec, Inc. v. Int’l Business Machines Corp.</i> , 731 F.3d 1336 (Fed. Cir. 2013) .....	8
<i>Teva Pharms. USA, Inc. v. Sandoz, Inc.</i> , 574 U.S. 318 (2015).....	14
<i>Trading Techs. Int’l, Inc. v. Open E Cry, LLC</i> , 728 F.3d 1309 (Fed. Cir. 2013) .....	26
<i>Uniloc USA, Inc. v. Apple, Inc.</i> , No. 19-cv-1692-EJD (VKD), 2021 WL 432183 (N.D. Cal. Jan. 15, 2021) .....	30
<i>Vitronics Corp. v. Conceptronic, Inc.</i> , 90 F.3d 1576 (Fed. Cir. 1996) .....	12
<i>Wasica Finance GmbH v. Continental Automotive Sys., Inc.</i> , 853 F.3d 1272 (Fed. Cir. 2017) .....	18, 27

## Rules

Fed. R. Evid. 702(b).....	14
---------------------------	----

## TABLE OF EXHIBITS<sup>1</sup>

Ex. No.	Description
1	U.S. Patent No. 9,529,768 (“768 patent”)
2	U.S. Patent No. 9,703,750 (“750 patent”)
3	U.S. Patent No. 8,977,797 (“797 patent”)
4	U.S. Patent No. RE44,654 (“654 patent”)
5	U.S. Patent No. RE45,140 (“140 patent”)
6	U.S. Patent No. 7,363,416
7	U.S. Patent No. 7,676,624
8	U.S. Patent No. 7,818,487
9	U.S. Patent No. RE41,294
10	U.S. Patent No. 8,041,873
11	U.S. Patent No. RE41,294
12	U.S. Patent No. RE41,961
13	U.S. Patent No. RE42,814
14	U.S. Patent No. RE42,984
15	U.S. Patent No. RE43,119
16	U.S. Patent No. RE43,171
17	U.S. Patent No. RE44,468
18	<i>ACQIS LLC v. ASUSTek Computer, Inc.</i> , 6:20-cv-966-ADA, Dkt. 64
19	<i>ACQIS LLC v. ASUSTek Computer, Inc.</i> , 6:20-cv-966-ADA, Dkt. 70
20	Declaration of Andrew Wolfe, Ph.D
21	<i>ACQIS LLC v. Samsung Elecs. Co.</i> , No. 2:20-cv-00295-JRG (E.D. Tex. Sept. 26, 2021), Dkt. 92
22	“Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,” TIA/EIA Standard, TIA/EIA-644 (Mar. 1996) (“ <i>TIA/EIA-644</i> ”)
23	“IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI),” IEEE Standards Board (March 21, 1996) (“ <i>IEEE 1596.3</i> ”)
24	“National Semiconductor LVDS Owner’s Manual” (1st Edition Spring 1997)
25	“National Semiconductor LVDS Owner’s Manual” (2nd Ed. Spring 2000)
26	Huq, S., et al., “An Overview of LVDS Technology,” Application Note 971 (Jul. 1998)

---

<sup>1</sup> For convenience, ACQIS reproduces the entirety of Defendants’ Table of Exhibits and adds new exhibits continuing Defendants’ numbering.

Ex. No.	Description
27	<i>ACQIS LLC v. Alcatel-Lucent USA Inc., et al.</i> (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129
28	<i>ACQIS LLC v. Alcatel-Lucent USA Inc., et al.</i> (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129-15 (Ex. N)
29	<i>ACQIS LLC v. Alcatel-Lucent USA Inc., et al.</i> (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129-14 (Ex. M)
30	<i>ACQIS LLC v. Alcatel-Lucent USA Inc., et al.</i> (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129-16 (Ex. O)
31	Ma, J., “A Closer Look at LVDS Technology,” Application Note 41
32	Patent Owner’s Preliminary Response, IPR2014-01469 (’814 Patent), Paper 7 (September 25, 2014)
33	Patent Owner’s Preliminary Response, IPR2014-01462 (’873 Patent), Paper 11 (December 15, 2014)
34	Institution Decision, IPR2014-01469 (’814 Patent), Paper 14 (March 11, 2015) [ <b><i>sic</i>, Institution Decision, IPR2014-01462 (’873 Patent), Paper 11 (March 11, 2015)</b> ]
35	Institution Decision, IPR2014-01462 (’873 Patent), Paper 11 (March 11, 2015) [ <b><i>sic</i>, Institution Decision, IPR2014-01469 (’814 Patent), Paper 14 (March 11, 2015)</b> ]
36	Excerpts from Hearing Transcript, IPR2014-01462; IPR2014-01469 (December 8, 2015)
37	Declaration of Robert Colwell, Ph.D
38	<i>ACQIS LLC v. EMC Corp.</i> , No. 1:14-cv-13560, Dkt. 185 (EMC Opening CC Brief)
39	Dep. Tr. of V. Lindenstruth Vol. 1 (EMC v. Acqis), IPR2014-01462, Exhibit 1028
40	ACQIS Preliminary Proposed Claim Constructions in <i>ACQIS LLC v. Sony Interactive Entertainment, LLC, et al.</i> , 6:22-cv-00386-ADA
41	<i>ACQIS LLC v. ASUSTek Computer, Inc.</i> , 6:20-cv-966-ADA, Dkt. 144 (Order Memorializing Whether Prior Constructions Apply to Terms in this Case)
42	Patent Owner’s Response, IPR2014-01469 (’814 Patent), Paper 25 (September 25, 2014)
43	IPR Decl. of V. Lindenstruth, IPR2014-01462 (’873 Patent), Ex. 2021 (EMC v. ACQIS)
44	Patent Owner’s Response, IPR2014-01462 (’873 Patent), Paper 30 (September 25, 2014)
45	PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998)
46	Universal Serial Bus Specification, Revision 2.0 (Apr. 27, 2000)
47	U.S. Patent No. 6,718,415
48 (New)	<i>ACQIS LLC v. Samsung Elecs. Co., Ltd., et al.</i> , No. 2:20-cv-00295-JRG, Dkt. 116 (E.D. Tex. Nov. 17, 2021) (“ <i>Samsung</i> , Dkt. 116”)

Ex. No.	Description
49 (New)	Expert Declaration of Nabil J. Sarhan, Ph.D. Regarding Claim Construction (June 9, 2023)
50 (New)	<i>VESA Plug &amp; Display Standard</i> Ver. 1, Rev. 0 (June 11, 1997) (“VESA P&D Standard”) <b>[HIGHLIGHTING ADDED]</b>
51 (New)	<i>Digital Visual Interface (DVI) Specification</i> , Rev. 1.0 (Apr. 2, 1999) (“DVI 1.0”) <b>[HIGHLIGHTING ADDED]</b>
52 (New)	HyperTransport Consortium Press Release (Apr. 2, 2001)
53 (New)	HyperTransport™ Technology I/O Link, A High-Bandwidth I/O Architecture, AMD White Paper (July 20, 2001) <b>[HIGHLIGHTING ADDED]</b>
54 (New)	<i>ACQIS LLC v. ASUSTeK Computer, Inc.</i> , No. 6:20-cv-966-ADA, Dkt. 124 (Transcript of Sept. 1, 2022 Hearing) (W.D. Tex. Sept. 2, 2022) <b>[HIGHLIGHTING ADDED]</b>
55 (New)	<i>ACQIS LLC v. ASUSTeK Computer, Inc.</i> , No. 6:20-cv-966-ADA, Dkt. 52 (Claim Construction Order) (W.D. Tex. Nov. 17, 2021)
56 (New)	<i>ACQIS LLC v. ASUSTeK Computer, Inc.</i> , No. 6:20-cv-966-ADA, Dkt. 115 (Transcript of July 13, 2022 Hearing) (W.D. Tex. July 14, 2022)
57 (New)	Universal Serial Bus Specification, Revision 1.0 (Jan. 15, 1996)



## I. INTRODUCTION

In parallel ACQIS proceedings, this Court has already considered and decided many of the parties' claim construction disputes here. In all such instances, ACQIS proposes constructions that adopt this Court's previous constructions. As to issue preclusion, this Court has already thoroughly considered and decided the impact of the claim construction and summary judgment rulings from the *ACQIS v. EMC* matter ("*EMC*")—involving different patents, terms, and claimed subject matter—and the Federal Circuit's affirmance, including how, if at all, the constructions from *EMC* apply to disputed terms in the Asserted Patents. Where applicable, ACQIS's proposed constructions adopt this Court's conclusions and reasoning.

Although the Defendants here are not bound by this Court's previous orders, Defendants fail to acknowledge the recent history of the Asserted Patents in previous and parallel ACQIS proceedings before this Court, much less explain why the Court should rule differently here on identical issues. ACQIS's claim construction proposals reflect and adopt this Court's previous constructions, which were the result of extensive work and consideration by this Court both before *and after* the Federal Circuit's decision in the *EMC* matter. ACQIS respectfully requests that the Court adopt its proposed constructions and decline to apply issue preclusion.

## II. THE ACQIS INVENTIONS

Dr. William Chu, the inventor of the ACQIS patents, made communications between computer components faster, more efficient, and less costly. He invented a new computer communication interface channel to replace the burdensome physical and electrical requirements of prior art computer buses such as the parallel Peripheral Component Interconnect (PCI) bus or the Universal Serial Bus (USB). Ex. 1, '768 at 3:23-4:16, 5:47-49, 25:8-12.<sup>2</sup> His inventions made

---

<sup>2</sup> As Defendants note, the '768, '750, and '797 patents largely share the same specification, and '654 and '140 patents share the same specification, which overlaps significantly with the

communication between computer components faster and more power-efficient while also reducing the number of wires and “pins” (electrical connections) needed. Dr. Chu’s new interface channel can still communicate certain information specified by prior industry specifications, such as PCI or USB, to maintain backwards compatibility with existing systems. Dr. Chu’s inventions enabled systems to preserve *what* information is communicated—such as address, data, or byte enable information—while improving *how* it is communicated—using Dr. Chu’s improved channel. Those inventions make computer systems faster, smaller, and more efficient.

Dr. Chu filed the utility applications leading to his patents in 1999 and 2000, and the ’768, ’750, and ’797 patents also claim priority to a provisional application filed in 1999. Claim construction thus must consider how a person of skill in the art (“POSITA”) would have understood the terms in this period. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005).

### **III. ISSUE PRECLUSION DOES NOT AFFECT THE ASSERTED CLAIMS**

Defendants raise the same issue preclusion arguments raised in Sony’s pending partial motion to dismiss, *see ACQIS, LLC v. Sony Interactive Entertainment, Inc., et al.*, No. 6:22-cv-386-ADA, Dkt. 24, and the same arguments rejected by this Court in co-pending ACQIS cases. The Court should reject Defendants’ issue preclusion arguments for the same reasons.

In *EMC*, the Federal Circuit affirmed constructions of different claim terms, from different patents, that the district court adopted based on agreements of the parties, the procedural posture of the case, and a finding that ACQIS forfeited its arguments on the merits. *ACQIS, LLC v. EMC Corp.*, No. 2021-1772, 2022 WL 1562847, at \*1 (Fed. Cir. May 18, 2022) (“*EMC Appeal Decision*”); *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2021 WL 1088207, at \*4-5 (D. Mass. Feb. 19, 2021) (“*EMC Summary Judgment*”). *See also* Ex. 21, *ACQIS LLC v. Samsung Elecs. Co.*,

---

’768/’750/’797 specification. For simplicity, in this brief ACQIS primarily cites the ’768 specification unless meaningful differences exist with the other patents.

*Ltd., et al. (“Samsung”)*, No: 2:20-cv-295-JRG, Dkt. 92 at 17-19 (E.D. Tex. Sept. 26, 2021). The *EMC Appeal Decision* therefore did not resolve, explicitly or by necessary implication, any issue of claim construction for the patents here, as the *Samsung* court found for the underlying *EMC* district court opinion. *Id.* at 17-19, 26.

The *EMC* district court and Federal Circuit did not hold “that transactions in accordance with the PCIe standards could not satisfy the claimed ‘PCI bus transaction,’ as construed.” Defs. Br. at 11. The *EMC* district court held that ACQIS forfeited its arguments about the import of the intrinsic record from different patents than the Asserted Patents, with different claims, and also did not dispute non-infringement except as to those forfeited arguments. The Federal Circuit affirmed the district court’s constructions without comment as to whether it affirmed as to the forfeiture or actually analyzed the intrinsic record for any particular patent claim.

Issue preclusion applies only to identical issues actually litigated and necessary to the judgment in a prior case. *State Farm Mut. Auto. Ins. Co. v. LogistiCare Sols., LLC*, 751 F.3d 684, 689 (5th Cir. 2014). *EMC* did not address the issues of claim scope presented in these cases.

**A. The Claim Scope Issues Here Are Not Identical to the Issues in *EMC*.**

The determination of the proper scope of the Asserted Claims here differ from the issues decided in *EMC*. It is not enough that the issues be similar or substantially the same—they must be *identical*. The Asserted Patents and claims in these cases do not overlap with *EMC. ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2017 WL 6211051, at \*1 (D. Mass. Dec. 8, 2017) (“*EMC Claim Construction*”) (listing asserted patents in *EMC*, all different than those asserted here).<sup>3</sup>

The claims at issue here differ from those in *EMC*. Defendants’ comparison of a claim from

---

<sup>3</sup> The patents asserted against Microsoft and Sony are identical to the patents asserted against Samsung. In *Samsung*, the Court considered whether the claim construction or summary judgment issues decided in *EMC* affected the same five Asserted Patents here and concluded they did not. Ex. 21, *Samsung*, Dkt. 92 at 18-19; Ex. 48, *Samsung*, Dkt. 116 (E.D. Tex. Nov. 17, 2021).

*EMC* (claim 38 of U.S. Patent No. 7,818,487 (“’487”)) and one from these cases (’797 claim 7) illustrates that they do not have identical scope. For example, ’487 claim 38 (*EMC*) recites “serial channels for transmitting *encoded PCI bus transaction data* in opposite directions.” Defs. Br. at 4 (citing Ex. 8) (emphasis added). In contrast, ’797 claim 7 recites “conveying *encoded address and data bits* of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the serial channels to preserve the PCI bus transaction.” Ex. 3, ’797 at 38:53-56 (emphasis added). These phrases have several differences, including that ’797 claim 7 recites “address and data bits of a” PCI bus transaction, and ’487 claim 38 does not. Defendants’ conclusory characterizations of the claims in *EMC* and these cases as “extremely similar,” “very closely related,” “extremely close,” and “highly similar,” Defs. Br. at 3-4, contradicted by their own example, all concede the same point: *EMC* addressed different issues of claim scope than the claims presented here.

**“PCI bus transaction”:** The term “PCI bus transaction” appears across the patents asserted in *EMC* and the Asserted Patents here but in different claim limitations with different scope. The *EMC* courts’ decisions thus do not inform or define the proper construction of different phrases reciting the term “PCI bus transaction” based on the claim language and disclosures of the different patents and claims asserted in this case.

For example, the *EMC* courts did not address the phrases at issue here reciting only certain bits of a “PCI bus transaction.” *EMC Claim Construction*, 2017 WL 6211051, at \*3-5, \*8; *EMC Summary Judgment*, 2021 WL 1088207, at \*3-6. The *EMC* courts also did not address, e.g., the teaching of Figure 8B, which illustrates the invention’s interface channel connected directly to a chip without a parallel PCI bus. *See* Ex. 1, ’768 at Fig. 8B. These differences in intrinsic evidence present different issues. *See Fenner Invs., Ltd. v. Cellco P’ship*, 778 F.3d 1320, 1322-23 (Fed. Cir. 2015) (“The terms used in patent claims are not construed in the abstract, but in the context in

which the term was presented and used by the patentee[.]”). *See also* Ex. 21, *Samsung*, Dkt. 92 at 18-19 (concluding, “where the EMC case involved claims of different scope in different patents asserted against different technology and where the *EMC Summary Judgment* was premised on the procedural posture rather than whether the PCI Local Bus Specification actually distinguishes between information used to convey a transaction and the transaction itself, collateral estoppel does not apply.”) (citing *State Farm*, 751 F.3d at 689).

**“Encoded” and “serial” phrases:** Neither the *EMC* district court nor the Federal Circuit addressed phrases at issue in this case reciting the terms “encoded” and/or “serial,” which all recite *only certain bits* of a “PCI bus transaction.” Instead, the *EMC* district court construed the phrase “[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction”—a phrase not present in the Asserted Claims here—“and related terms.” *EMC Claim Construction*, 2017 WL 6211051, at \*5-8; *EMC Summary Judgment*, 2021 WL 1088207, at \*5-6. The Federal Circuit, accordingly, affirmed the construction of the same phrase. *EMC Appeal Decision*, 2022 WL 1562847, at \*1. The Federal Circuit did not address the different claim language in the present cases. Finally, this Court in *ACQIS LLC v. ASUSTeK Computer Inc.*, No. 6:20-cv-966-ADA (W.D. Tex.) (“*ASUSTeK*”), assessed the impact of *EMC* on the “encoded” and “serial” phrases at issue in the present cases, as discussed below. *See* Ex. 41, *ASUSTeK*, Dkt. 144 at 2.

**“Communicating . . . PCI bus transaction”:** The phrase “communicating . . . PCI bus transaction” from *EMC*, without reference to specific recited bits being communicated, does not appear in any of the Asserted Claims here. The district court in *EMC* did not decide whether to provide different constructions for “communicating” phrases reciting an “entire” “PCI bus transaction” and phrases reciting only certain “bits” of a “PCI bus transaction.” The parties in *EMC* did not present this issue as a dispute—instead, they agreed to a construction of “communicating

. . . PCI bus transaction”: “communicating a PCI bus transaction, including all address, data, and control bits.” *EMC Claim Construction*, 2017 WL 6211051, at \*8. The *EMC* courts thus did not address whether different “communicating” phrases should have different constructions, *id.*, as this Court concluded they should in *ASUSTeK*. Ex. 41, *ASUSTeK*, Dkt. 144 at 2.

**“Bits” phrases:** Neither the *EMC* district court nor the Federal Circuit addressed the claim language at issue here reciting specific bits of a “PCI bus transaction”: either “address and data bits” or “address bits, data bits, and byte enable information bits.” *EMC Claim Construction*, 2017 WL 6211051, at \*3-5, \*8; *EMC Summary Judgment*, 2021 WL 1088207, at \*3-6; *EMC Appeal Decision*, 2022 WL 1562847, at \*1. The district court’s and Federal Circuit’s opinions therefore provide no guidance or direction as to these terms. None of the phrases described by the Federal Circuit as “slight variations” recite only certain “bits” of a “PCI bus transaction”—they *all* recite an entire “PCI bus transaction.” *EMC Appeal Decision*, 2022 WL 1562847, at \*1 n.1.

Finally, the cases relied on by Defendants do not apply here because they address identical claim terms in the same claim context. *In re Rambus Inc.*, 694 F.3d 42, 48 (Fed. Cir. 2012) (“[T]he same claim term in the same patent or related patents carries the same construed meaning.”) (quotation omitted); *SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (“Where multiple patents derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.”) (quotation omitted); *Abtox, Inc. v. Exitron Corp.*, 131 F.3d 1009, 1010 (Fed. Cir. 1997) (“Although these claims have since issued in separate patents, it would be improper to construe this term differently in one patent than another, given their common ancestry.”). *Ohio Willow Wood*, cited by Defendants, states that an application of collateral estoppel to previously un-litigated patent claims is only appropriate “[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not

materially alter the question” at issue. *Ohio Willow Wood Co. v. Alps South, LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013). The claims at issue in *EMC* and the Asserted Claims here use different phrases with different scope, as discussed above, and thus “materially alter” the issues.

**B. The Issues of Claim Scope Here Were Not Actually Litigated or Necessary to the Judgment in *EMC*.**

In *EMC*, the parties agreed to the construction of “PCI bus transaction.” *EMC Claim Construction*, 2017 WL 6211051, at \*3 (discussing language agreed to by the parties), \*5 (adopting language). The district court did not evaluate the intrinsic record to determine which aspects of the PCI Local Bus Specification (“PCI Specification”) the claims required except to determine that the phrase does not require a physical PCI bus. *Id.* at \*3-5.

A stipulated construction does not resolve the issue, under the *Phillips* standard, of how a POSITA would have understood the term in view of the intrinsic evidence. *See Pfizer, Inc. v. Teva Pharms. USA, Inc.*, 429 F.3d 1364, 1375-76 (Fed. Cir. 2005) (refusing to apply issue preclusion based on stipulated construction, from prior case, to the same patent claims in later case, and instead analyzing the evidence under *Phillips*); *Allergan Sales, LLC v. Sandoz Inc.*, No. 2:12-cv-207-JRG, 2016 WL 1224868, at \*5-7 (E.D. Tex. Mar. 29, 2016) (finding that issue preclusion did not arise from stipulated construction). The construction of “PCI bus transaction” under *Phillips* was neither litigated nor decided in *EMC*.

At summary judgment in *EMC*, the parties disputed the meaning of their agreed construction. *EMC Summary Judgment*, 2021 WL 1088207, at \*3-5. EMC argued that the construction required a transaction “in accordance with every element of the Specification”; ACQIS argued that the construction required only certain elements of the PCI Specification. *Id.* at \*4. The district court found that ACQIS had forfeited any opposition to the claim scope asserted by EMC. *Id.* at \*4-5 (finding that “ACQIS’s attempt to reduce the import of the Specification is

untimely” and “[t]here is no need to now construe a readily understandable term that ACQIS itself thought clear when offering proposed constructions of related terms and the Court will not do so.”). *EMC* thus addressed different issues from the claim construction issues here, i.e., (1) interpretation of the parties’ stipulated construction for “PCI bus transaction”; and (2) whether ACQIS forfeited its arguments about the interpretation of the stipulated construction. *Id.* at \*3-6.

The *EMC* district court further found that ACQIS did not dispute non-infringement under EMC’s interpretation of the agreed construction and thus granted summary judgment. *Id.* at \*5. The district court also addressed the claim terms “encoded . . . serial bit stream of [PCI] bus transaction and related terms” and “communicating . . . PCI bus transaction.” *Id.* at \*5-6. It found that the scope of “PCI bus transaction” justified summary judgment of non-infringement for these terms as well. *Id.* at \*6 (“This Court has already concluded that the claims are limited by the Specification in its entirety. Therefore, for the reasons described above, there is no infringement, and summary judgement is appropriate.”). The district court made no findings about whether different constructions could apply to different “communicating” phrases under *Phillips*. *Id.* at \*6.

The Federal Circuit’s affirmance in May 2022 does not change the issue preclusion analysis. The Federal Circuit did not analyze any term under *Phillips*, and it did not state the basis for its adoption of the district court’s constructions. *EMC Appeal Decision*, 2022 WL 1562847, at \*1. Its opinion neither explicitly nor implicitly resolves the legal issue of the proper construction of any term under *Phillips*, because it does not explain whether it affirmed the district court’s constructions based on the procedural posture of the case and a forfeiture finding. *See TecSec, Inc. v. Int’l Business Machines Corp.*, 731 F.3d 1336, 1341-42 (Fed. Cir. 2013) (explaining that Federal Circuit decisions bind lower courts only for issues decided either explicitly or “by necessary implication,” and alternative potential grounds for affirmance preclude a finding of necessary



implication for either ground).

ACQIS's claims against Microsoft and Sony present issues of (1) the proper scope of the patent claims, which were not asserted or addressed in *EMC*; and (2) infringement by Microsoft and Sony products under that claim scope. These issues were neither litigated nor addressed by the district court or Federal Circuit in *EMC*, and therefore issue preclusion does not apply.

Consistent with this Court's previous rulings, because these cases involve non-identical issues—different patents, terms, and claim scope—to those at issue in *EMC*, and *EMC* involved numerous issues not fully and vigorously litigated, collateral estoppel does not apply.

#### IV. CLAIM CONSTRUCTION

##### A. “low voltage differential signal (LVDS) [channel]” / “LVDS [channel]”

'797 claims 7, 14, 33, 34, 36; '768 claims 1, 2, 4, 13, 17, 39, 40; '750 claims 1, 2, 5, 7, 10, 12, 21, 24, 31, 34, 35, 44; '654 claim 20, 21, 23, 26, 35; '140 claim 14, 15, 17-19, 21, 30, 31, 34-36, 38	
ACQIS's Construction	Defendants' Construction
No construction necessary. These terms should be given their plain and ordinary meaning.	“[a channel for carrying] a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3,” or, alternatively, indefinite.

For the first time in the litigations involving the Asserted Patents, Defendants have argued that a POSITA would interpret the term “LVDS” as either limited to two specific standard specifications or completely subjective and indefinite. Defendants are wrong on both counts. The plain descriptions of “LVDS” in the intrinsic record demonstrate that the term had a known, generic, objective meaning to a POSITA in 1998-1999. The term needs no construction.

In 1998-1999, “LVDS” had an objective, known meaning to those of skill in the art. Ex. 49, Sarhan Decl., ¶¶ 32, 42. A POSITA would have understood that “LVDS” refers to a differential signaling technique that allowed a voltage swing lower than prior data transmission standards,

such as ECL and PECL. *Id.*, ¶ 42; Ex. 26, Huq, at 1-2. The ACQIS specifications explain they use “LVDS” according to its ordinary, generic meaning not limited to any specific LVDS technology:

It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. *The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.*

Ex. 1, '768 at 4:9-16 (emphasis added); Ex. 2, '750 at 4:11-18; Ex. 3, '797 at 3:65-4:5; Ex. 49, Sarhan Decl., ¶ 34.

The ACQIS specifications also describe a specific example of LVDS technology:

P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard . . . . *TMDS stands for Transmission Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology.* TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

Ex. 1, '768 at 21:25-36 (emphasis added); Ex. 2, '750 at 21:23-34; Ex. 3, '797 at 20:43-54; Ex. 4, '654 at 21:9-19; Ex. 5, '140 at 21:13-23; Ex. 49, Sarhan Decl., ¶¶ 36, 48. The Asserted Patents' cited art includes the 1997 *VESA Plug & Display Standard*, to which the quote above refers. *See, e.g.*, Ex. 1, '768 at p. 11. That reference confirms that “LVDS” had a recognized, generic meaning at that time—it defines “LVDS” as “Low Voltage Differential Signaling” and explains:

*The term LVDS is used in this document as a generic term and does not imply any particular LVDS technology.*

Ex. 50, VESA P&D Standard, at 4 (emphasis added); Ex. 49, Sarhan Decl., ¶¶ 35 45. That art describes a type of LVDS, called “Transition Minimized Differential Signaling” or “TMDS,” not tethered to any specific LVDS standard. Ex. 50, VESA P&D Standard, at 31-33; Ex. 49, Sarhan Decl., ¶ 37. The VESA P&D Standard requires compliance with many industry standards, but not

any relating to LVDS, further demonstrating that “LVDS” had a recognized generic meaning not limited to specific standards. Ex. 50, VESA P&D Standard, at 5; Ex. 49, Sarhan Decl., ¶ 38.

Extrinsic evidence also confirms that “LVDS” had a recognized generic meaning in 1999 that persisted later. The *Digital Visual Interface (DVI) Specification*, Rev. 1.0 (Apr. 2, 1999) (“DVI 1.0”) explains that “T.M.D.S. technology uses current drive to develop the *low voltage differential signal* at the receiver side of the DC-coupled transmission line.” Ex. 51, DVI 1.0 at 33 (emphasis added). The members of the Digital Display Working Group, which published the DVI specification, include well-known industry leaders Intel, Compaq, Fujitsu, Hewlett-Packard, IBM, and NEC. *Id.* at 2. Materials published by AMD in 2001 describing a technology called “HyperTransport” explain that HyperTransport used “a type of low voltage differential signaling (LVDS),” but “not the conventional IEEE LVDS standard,” further confirming the industry’s understanding of the generic term “LVDS.” Sarhan Decl., ¶¶ 40-41; Exs. 52, 53.

The Asserted Patents thus use the term “LVDS” according to a generic meaning known to those of skill in the art in 1998-1999. Defendants and Dr. Wolfe, however, contend a POSITA would understand “LVDS” to refer to only two specific standards or not understand it at all.

A POSITA in 1998-1999 would not have limited the generic term “LVDS” to the two specific standards relied on by Defendants, TIA/EIA-644 and IEEE 1596.3, as demonstrated by the evidence above. Ex. 49, Sarhan Decl., ¶ 46. The mere existence of two different standards both describing “LVDS” indicates that “LVDS” had a more generic meaning than the specific technologies in either standard. *Id.*, ¶ 47.

The specification’s specific reference to TMDS as “LVDS technology” contradicts Defendants’ construction limited to two specific standards. A POSITA would recognize that TMDS does not follow either TIA/EIA-644 or IEEE 1596.3. *Id.*, ¶ 49.

Neither Defendants nor Dr. Wolfe address this plain contradiction between their interpretation of “LVDS” and the intrinsic evidence. They do not address the Asserted Patents’ description of TMDS LVDS technology at all. Dr. Wolfe catalogs “exemplary disclosures” regarding LVDS from the Patents’ specification and includes nearly all references to “LVDS” *except* the identification of TMDS, which plainly renders his opinions incorrect. Ex. 20, Wolfe Decl., ¶ 40. Defendants’ narrow construction would violate fundamental claim construction law by excluding the TMDS embodiment of “LVDS” technology. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (finding that a construction that excludes an embodiment is “rarely, if ever, correct”).

Defendants and Dr. Wolfe also misinterpret statements from industry references that they contend “define” “LVDS.” They point to two related statements: “two key industry standards define LVDS,” and “[t]here are two industry standards that define LVDS.” Defs. Br. at 8-9; Ex. 20, Wolfe Decl., at ¶¶ 31-34. A POSITA would recognize, in view of the evidence above, that these statements indicate that the two standards “define” specific *types* of LVDS, not that they define *every* kind of “LVDS” technology, which plainly has a broader meaning in view of TMDS. Ex. 49, Sarhan Decl., ¶ 33.

Defendants’ and Dr. Wolfe’s failure to recognize TMDS as an example LVDS technology also undermines their argument that a POSITA would not have understood the meaning of “LVDS” with reasonable certainty without reference to TIA/EIA-644 and IEEE 1596.3. As shown above, industry literature, cited in the Asserted Patents (and thus intrinsic evidence), recognized “LVDS” as a “generic term,” not limited to two specific standards. That VESA, the Video Electronics Standards Association, understood and could implement “LVDS” as a “generic term” indicates that a POSITA would have understood its scope with reasonable, if not absolute,

certainty. Ex. 50, VESA P&D Standard, at 4-5, 31-33; Ex. 49, Sarhan Decl., ¶¶ 50-52. Defendants and Dr. Wolfe do not address this.

The evidence above demonstrates that “low voltage” does not require “a subjective determination,” as Dr. Wolfe contends, or represent “a subjective term of degree,” as Defendants contend. Ex. 20, Wolfe Decl., ¶ 38; Defs. Br. at 10. The art cited in the Asserted Patents and extrinsic evidence demonstrates that a POSITA understood that “LVDS” utilized lower voltage than existing data transmission techniques, and industry giants used the term accordingly. This understanding provides an objective boundary for “LVDS” that a POSITA could apply without a subjective determination. Determining whether a particular accused product or asserted prior art reference implements “LVDS” requires an objective, factual application of the term’s known usage, not a subjective opinion.

In view of this evidence, and Defendants’ and Dr. Wolfe’s failure to address it, Defendants have not established, by clear and convincing evidence, that a POSITA would not understand the term “LVDS” in the Asserted Patents with reasonable certainty. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901, 910 (2014). The use of “LVDS” as a generic term, without reference to a specific standard, by companies such as Intel, AMD, HP, and IBM shows that “LVDS” is not a subjective term of degree, and indicates that the term provides sufficient notice to those of skill in the art about the scope of ACQIS’s claims. *See One-E-Way, Inc. v. Int’l Trade Comm’n*, 859 F.3d 1059, 1063 (Fed. Cir. 2017) (explaining that superficially “relative” terms do not render claims indefinite where those skilled in the art recognize their meaning) (applying *Nautilus* and *Eibel Process Co. v. Minn. & Ontario Paper Co.*, 261 U.S. 45, 65-66 (1923)). The weight of the evidence favors ACQIS’s position that “LVDS” had a well-understood, ordinary, objective meaning in 1998, and the term needs no construction.

Dr. Wolfe’s failure to address the ACQIS specifications’ description of TMDS, and the corresponding description of “LVDS” as a “generic” term in the VESA reference describing TMDS (also intrinsic evidence, as cited art), undermines the credibility of his indefiniteness opinions and renders them unreliable for failure to consider “sufficient facts or data.” Fed. R. Evid. 702(b). Defendants rely on no other evidence to establish that a POSITA would have found the term “LVDS” subjective if not limited to two example standards—a question of fact. *See Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 327, 331-32 (2015) (recognizing the meaning of a term in the art as an issue of fact). Defendants thus have not established indefiniteness by any evidence, and certainly not clear and convincing evidence. *Cox Commc’ns, Inc. v. Sprint Commc’n Co. LP*, 838 F.3d 1224, 1228 (Fed. Cir. 2016) (“Any fact critical to a holding on indefiniteness . . . must be proven by the challenger by clear and convincing evidence.” (internal quotation omitted)).

**B. “Peripheral Component Interconnect (PCI) bus transaction” / “PCI bus transaction”**

’797 claims <u>7</u> , <u>14</u> , <u>36</u> , <u>38</u> ; ’768 claims <u>1-5</u> , <u>13</u> , <u>14</u> , <u>17</u> , <u>39</u> ; ’750 claims <u>1-3</u> , <u>5</u> , <u>7</u> , <u>10</u> , <u>12</u> , <u>21</u> , <u>31-33</u> , <u>34</u> , <u>35</u> , <u>44</u> , <u>45</u> ; ’654 claim <u>21</u> , <u>24</u> , <u>26</u> , <u>35</u> ; ’140 claim <u>30</u> , <u>31</u> , <u>34</u> <sup>4</sup>	
ACQIS’s Construction	Defendants’ Construction
“a transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component”	“a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component”

The term “PCI bus transaction” has been construed multiple times throughout the history of ACQIS litigation. Most recently, this Court revisited its construction of “PCI bus transaction” in the *ASUSTeK* matter in view of the Federal Circuit’s decision in *EMC*. This Court concluded

---

<sup>4</sup> In some instances, Defendants have listed dependent claims from the Asserted Patents that do not recite the disputed claim terms. For clarity, in such instances, ACQIS has underlined claims where the disputed terms explicitly appear.

that “in accordance with” includes “backward compatibility” and that adding “backwards compatibility” does not expand the claim scope. Ex. 54, *ASUSTeK*, Dkt. 124 (Transcript of Sept. 1, 2022 Hearing) at 36:6-16 (W.D. Tex. Sept. 2, 2022). The parties’ only dispute over this term is the inclusion of the clarifying language “*or backwards compatible*.”

**1. “Backwards Compatible” Does Not Conflict with the Federal Circuit’s Decision in *EMC*.**

In *EMC*, the district court construed “PCI bus transaction” as “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” *EMC Claim Construction*, 2017 WL 6211051, at \*5. The Federal Circuit affirmed. *EMC Appeal Decision*, 2022 WL 1562847, at \*1.

Separately, in September 2021 in *Samsung*, the court construed the term the same way, but explicitly declined to specify “what set of information qualifies as a transaction under the PCI Local Bus Specification,” (Ex. 21, *Samsung*, Dkt. 92 at 17-18), concluding that “[w]hether a particular set of information meets that standard [i.e., the PCI Local Bus Specification] is properly left be [sic] determined in the context of infringement or invalidity.” *Id.* at 19.

Shortly thereafter, in November 2021 in *ASUSTeK*, this Court construed “PCI bus transaction” as “a transaction, in accordance *or backwards compatible* with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” Ex. 55, *ASUSTeK*, Dkt. 52 at 4 (W.D. Tex. Nov. 17, 2021) (emphasis added).

After the Federal Circuit affirmed the district court’s decision in *EMC*, several defendants sought to apply the *EMC* constructions to terms at issue in cases before this Court. In a July 13, 2022 hearing, this Court addressed the impact of the Federal Circuit’s decision in *EMC*. Ex. 56, *ASUSTeK*, Dkt. 115 (Transcript of July 13, 2022 Hearing) (W.D. Tex. July 14, 2022). The Court then ordered the parties to specifically address the “or backwards compatible” language, *id.* at

66:8-21, and the parties in those matters submitted supplemental briefing to address the issue. *See ASUSTeK*, No. 6:20-cv-966-ADA, Dkts. 116-119.

The Court held another hearing on September 1, 2022. Regarding “PCI bus transaction,” this Court stated that although it was “adopt[ing] the [Federal] Circuit’s construction of ‘a transaction in accordance with the industry standard PCI local bus specification [f]or communication with [an] interconnected peripheral component,’” the Court was also “putting on the record—and we’ll get a written order out on this as quickly as possible—we agree with plaintiff [ACQIS] that ‘in accordance with’ includes ‘backward compatibility’ and that adding ‘backwards compatibility’ does not expand the claim scope.” Ex. 54, *ASUSTeK*, Dkt. 124 at 36:6-16.

This Court has thus already analyzed the “backwards compatible” issue in considerable depth, based on the same arguments Defendants make here, and concluded that “in accordance with” includes “backwards compatibility” and that adding “backwards compatibility” does not expand claim scope and does not conflict with the construction from *EMC*. *Id.* ACQIS’s proposed construction adopts this Court’s ruling. Although ACQIS’s proposal includes “or backwards compatible” for clarity to address the parties’ apparent dispute over the meaning of “in accordance with,” it would also be appropriate to adopt the construction that excludes “or backwards compatible” but provide further clarification, as the Court did in *ASUSTeK*, that “in accordance with” in the construction includes backwards compatibility. *See* Ex. 49, Sarhan Decl., ¶¶ 57-58.

## **2. The Intrinsic Record Supports “Backwards Compatible.”**

“Backwards compatible” is supported by the intrinsic record. Although the words “backwards compatible” do not appear in the Asserted Patents, the concept of backwards compatibility does. Ex. 49, Sarhan Decl., ¶¶ 59-60. The invention replaces the parallel wiring and corresponding control signals used for parallel data transmission with an interface that communicates information serially over LVDS channels and maintains compatibility with the prior



art PCI bus. Ex. 1, '768 at 5:47-6:11; 6:41-52; Ex. 49, Sarhan Decl., ¶¶ 61-63. The specification describes a particular embodiment of the invention, referred to as the “XPBus,” that receives and transmits “PCI address and data” information (Ex. 1, '768 at 18:11-27), and “may be used to interface two PCI or PCI-like buses . . . .” *Id.* at 18:50-62. Many embodiments have no parallel PCI bus and replace that architecture with serial architecture. *See, e.g., id.* at Figs. 8A, 8B (showing invention’s LVDS channel “directly connected” to a chip with no parallel PCI Bus). Three courts have construed the claims as not requiring a PCI bus. *See* Ex. 55, *ASUSTeK*, Dkt. 52 at 4; *EMC Claim Construction*, 2017 WL 6211051, at \*4-5; *ACQIS, LLC v. Appro Int’l, Inc.*, No. 6:09-cv-148, 2011 WL 382556, at \*5-6 (E.D. Tex. Feb. 3, 2011) (“*Appro*”).

Judge Davis of the Eastern District of Texas recognized backwards compatibility, finding that “the ‘PCI bus transaction’ allows compatibility with PCI legacy devices when replacing the conventional parallel PCI bus with a serial architecture.” *Appro*, 2011 WL 382556, at \*6. Judge Davis further stated that “one of skill in the art would conclude that the term PCI bus in the patent is not specific to a PCI Local Bus Standard form of architecture and that a ‘PCI bus transaction’ is used to merely designate[] an ability to communicate with a legacy device . . . so that backward compatibility with an installed base of peripherals is assured.” *Id.* at \*6. Judge Davis thus acknowledged that the inventions provide a new bus architecture, not limited solely to the PCI Local Bus Specification, that can achieve backwards compatibility with legacy PCI devices.

### **3. ACQIS’s Proposed Construction Is Consistent with ACQIS’s Previous Statements to the PTAB and *EMC* District Court.**

ACQIS’s statements to the PTAB have no bearing on the inclusion of “or backwards compatible” in the construction of “PCI bus transaction.” This Court has already concluded that “or backwards compatible” does not expand the claim scope and that “in accordance with” includes “backward compatibility.” Ex. 54, *ASUSTeK*, Dkt. 124 at 36:6-16. “Backwards compatibility” is

consistent with the intrinsic record, as discussed above. ACQIS’s statements in IPR that, e.g., a “PCI bus transaction” is a “bus transaction in accordance with the Peripheral Component Interconnect protocol,” (Ex. 32, ’814 IPR Prelim. Resp. at 7), change nothing.

**C. “convey [/conveying/conveys/communicating/communicate/transmitting] ... a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]”**

<b>'797 claims <u>7</u>, <u>14</u>, <u>36</u>, <u>38</u>; '768 claims <u>1-5</u>, <u>13</u>, <u>14</u>, <u>17</u>, <u>39</u>; '750 claims <u>1-3</u>, <u>5</u>, <u>7</u>, <u>10</u>, <u>12</u>, <u>21</u>, <u>31-33</u>, <u>34</u>, <u>35</u>, <u>44</u>, <u>45</u>; '654 claim <u>21</u>, <u>24</u>, <u>26</u>, <u>35</u>; '140 claim <u>30</u>, <u>31</u>, <u>34</u></b>	
<b>ACQIS’s Construction</b>	<b>Defendants’ Construction</b>
Other than “PCI bus transaction,” addressed above, these terms do not require construction.	“communicating a PCI bus transaction, including all address, data, and control bits”

Defendants’ framing of this issue is aimed at bringing the Asserted Claims within the scope of *EMC*. Unlike the claims addressed substantively in *EMC*, however, every Asserted Claim that references a PCI bus transaction specifies the bits *actually* conveyed: either “address and data [bits] of a Peripheral Component Interconnect (PCI) transaction” or “address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) transaction.”

Defendants seek to discard the express claim language<sup>5</sup> and construe all “PCI bus transaction” claims, no matter which bits they recite, as requiring “a PCI bus transaction, including all address, data, and control bits.” Defendants’ proposed construction plainly conflicts with the claim language and improperly renders it meaningless. *See Wasica Finance GmbH v. Continental Automotive Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”). It also conflicts with the specifications’ disclosures to the extent the construction requires *all* control signals used

---

<sup>5</sup> Defendants’ proposed construction also unnecessarily replaces easily understood terms such as “convey[ing]” and “transmit[ing]” with “communicating.” There is no reason to rewrite the claims in the manner Defendants propose. None of these terms require construction.

for a prior art parallel PCI bus, because it would exclude the embodiments that do not have a physical, parallel PCI bus requiring those signals. *See* Ex. 1, '768 at Figs. 8A, 8B; *Eko Brands, LLC v. Adrian Rivera Maynez Enters., Inc.*, 946 F.3d 1367, 1373 (Fed. Cir. 2020) (refusing to adopt proposed construction that would exclude embodiments).

Defendants first contend that because ACQIS agreed to Defendants' construction in *EMC*, that construction should apply here. Not so. A claim construction adopted by stipulation in one case does not have preclusive effect in a later case. *See Pfizer*, 429 F.3d at 1375-76 (refusing to apply stipulated construction, from prior case, to same patent claims in later case). Further, the parties' agreement in *EMC* is inapplicable here because it related to different patents, terms, and claim scope. *See* § III, *supra*.

Defendants next contend that “[t]here can be no specific bits of a PCI bus transaction without an actual ‘PCI bus transaction’” and accuse ACQIS of “read[ing] the language ‘of a PCI bus transaction’ out of the claims[.]” Defs. Br. at 15. Defendants are incorrect, and limitations reciting conveying specific bits do not require the existence of an entire PCI bus transaction, as discussed in § IV.D, *infra*, regarding the disputed “of a [PCI bus transaction]” term.

### **1. IPR Disclaimer Does Not Apply to the Asserted Claims.**

Defendants contend that IPR disclaimer applies and supports their construction. Defendants contend various statements by ACQIS's counsel in IPR proceedings—relating to different patents—support Defendants' constructions. *See* Defs. Br. at 16 (citing Ex. 36, IPR Hr'g Tr. at 35:11-17, 38:7-17, 38:18-20, 49:13-14, 50:12-16).

Defendants mischaracterize both what was said and the import of what was said. First, the statements by counsel were in the context of claims that differ in significant ways from the Asserted Claims here. *See* §III, *supra*. ACQIS's IPR counsel was referring to '873 claim 54 (or in

some instances, dependent claim 61),<sup>6</sup> which requires conveying an entire PCI bus transaction, and not specific, recited bits like the Asserted Claims. *See* Ex. 10, '873 at 43:40-52 (reciting serial bit channels “for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction”). As Judge Payne noted in *Samsung* about '873 claim 54,<sup>7</sup> “the claim requires the all information of a PCI bus transaction,” and “[t]he patent owner’s statements during IPR must be interpreted in this context.” Ex. 21, *Samsung*, Dkt. 92 at 22. Judge Payne concluded that ACQIS’s counsel’s statements in IPR “do[] not rise to the level of disclaimer to constrain a list of information items from a PCI bus transaction to require all information of a PCI bus transaction regardless of what items are enumerated in the list.” *Id.* at 23.

Second, the parties in *EMC* disagreed about the meaning of “control bits.” ACQIS used the term to mean PCI command bits, while EMC interpreted it to mean PCI bus control *signals* (as opposed to “bits”). In IPR, ACQIS’s counsel used “control bits” to refer to command bits:

*And in the address phase they send the address and the control bits. So during that phase the control bit, if it’s an interrupt acknowledge, you can see that the address bits are don’t cares.*

Ex. 36, IPR Hr’g Tr. at 37:24-38:2 (emphases added). This statement aligns with the PCI Specification’s explanation that “[d]uring the address phase of a transaction, C/BE[3::0]# define the bus *command*[.]” Ex. 45, PCI 2.2 at 9-10 (emphasis added). It further explains that “Interrupt Acknowledge” is a “Command Type” defined by the value “0000” for the bits C/BE[3::0]#. *Id.* at 21. ACQIS’s counsel therefore did not describe the invention, even for the different patents at issue in IPR, in a way that requires PCI *signals* needed for a prior art PCI bus.

Defendants also mischaracterize statements of ACQIS’s IPR expert, Dr. Lindenstruth.

---

<sup>6</sup> No quoted statement by ACQIS’s IPR counsel is related to '814 claim 24. *See generally* Ex. 36.

<sup>7</sup> Regarding '873 claim 61, which depends from claim 54, Judge Payne noted, “Claim 61 excludes from the scope of the claim the interrupt acknowledge transaction by requiring non-zero address bits.” Ex. 21, *Samsung*, Dkt. 92 at 23.

Defs. Br. at 16-17. Dr. Lindenstruth did not say that “*control bits* ‘define the transaction,’” as Defendants claim. *Id.* at 16 (emphasis added). Defendants point to no testimony where Dr. Lindenstruth discussed “control bits” at all. Dr. Lindenstruth described sending PCI transactions *on a PCI bus*, and in that context, he refers to “control signals” sent over “control lines” *not* “control bits.” Ex. 39, V. Lindenstruth Dep. Tr. at 145:18-146:17. Dr. Lindenstruth’s statements about “control lines” and “control signals” referred to passages from the PCI Specification describing the use of a physical PCI bus. *See, e.g., id.* at 146:4-9 (“Q. . . . Are these control lines also part of what the claims require as a PCI bus transaction. A. Since they [control lines] are required to define *what is going on on the bus* at any point in time, the answer is yes. They define the PCI transaction.” (emphasis added)). No Asserted Claims here recite a physical PCI bus.

Even if the control lines (not control bits) “define the transaction” in the context of a physical PCI bus, that does not mean they are *part of* the “transaction.” Dr. Lindenstruth’s testimony indicates they are separate:

The frame signal is there to define the length of the transaction. This is a very fundamental thing because, unlike in other cases, in particular typically in networks, where the length of the packet is basically submitted as one of the very first words in the head of the packet saying, “This is it” and, “This is how long it will be.” In PCI this doesn’t exist.

*Id.* at 143:9-16. Whereas in some protocols, the length of a transaction is submitted as part of the transaction/packet, Dr. Lindenstruth testified that is not the case with PCI. *Id.* A protocol can require sending a message on one wire saying “the next packet you see will be three bytes long” and then send the packet/transaction on another, different wire. The first message is not a “part” of the “transaction” even if it does “have to be there” (as when conveying a PCI bus transaction over a parallel bus) and “defines the transaction.”

Further, Dr. Lindenstruth’s statement that “command information” is “other corollary information . . . needed to define a PCI transaction,” (*id.* at 121:5-17), has no bearing on whether

the Asserted Claims require, e.g., “control bits,” as Defendants’ construction would require.

Dr. Lindenstruth’s testimony regarding how PCI bus transactions are conveyed over a physical PCI bus does not constitute an unequivocal disclaimer of claim scope for the *EMC* claims or the different Asserted Claims here. *See Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016) (finding ambiguous statement does not constitute unequivocal disclaimer).

**2. The Specifications of the Asserted Patents Do Not Show Control Bits Being Part of a PCI Bus Transaction.**

Defendants mischaracterize the specifications of the Asserted Patents to require control bits as part of a PCI bus transaction. Defs. Br. at 18. The ’768 specification illustrates “PCI bus transaction” without requiring any parallel PCI control signals. First, “BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus,” and they indicate XPBus functions like “idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.” Ex. 1, ’768 at 21:40-47, 21:59-63. These bits, BS0 to BS3, represent new status information for the invention’s new interface channel, not PCI signals.

Second, in “one embodiment,” BS0-BS3 represent “*part of the function* of PCI control signals, *such as* FRAME#, IRDY#, and TRDY#.” *Id.* at 21:37-58 (emphases added). That is, BS0-BS3 do not represent *all* control signals, and they may or may *not* represent FRAME#, IRDY#, and TRDY#, as indicated by the permissive exemplary language “such as.” If BS0-BS3 present a PCI signal at all, they need not represent *all* the functionality of any signal. Similarly, again in “one embodiment,” “BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively.” *Id.* at 22:31-32. That is, BS0-BS3 may, but not *must*, represent PCI control signals.

**D. “of a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]”**

<p><b>’797 claims <u>7</u>, <u>14</u>, <u>36</u>, <u>38</u>; ’768 claims <u>1-5</u>, <u>13</u>, <u>14</u>, <u>17</u>, <u>39</u>; ’750 claims <u>1-3</u>, <u>5</u>, <u>7</u>, <u>10</u>, <u>12</u>, <u>21</u>, <u>31-33</u>, <u>34</u>, <u>35</u>, <u>44</u>, <u>45</u>; ’654 claim <u>21</u>, <u>24</u>, <u>26</u>, <u>35</u>; ’140 claim <u>30</u>, <u>31</u>, <u>34</u></b></p>
---

ACQIS's Construction	Defendants' Construction
No construction necessary. Putting aside “PCI bus transaction,” addressed above, this phrase should be broadened to include its full context—i.e., “address and data [bits] of a Peripheral Component Interconnect (PCI) bus transaction” / “address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction”—and given its plain and ordinary meaning.	“from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communicating with an interconnected peripheral component”

Defendants seek to reword otherwise clear claim language “of” to “from,” and construe the remainder of the phrase largely according to their proposed construction of “PCI bus transaction.” Defendants’ proposed construction is unnecessary and incorrect and should not be adopted.

First, Defendants’ proposed term beginning with “of a” removes context, namely the specific recited bits of a PCI bus transaction. In each instance of “of a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction],” the language is preceded by specific bits: either “*address and data [bits]* **of a** Peripheral Component Interconnect (PCI) transaction” or “*address bits, data bits, and byte enable information bits* **of a** Peripheral Component Interconnect (PCI) transaction.” If these terms are to be construed, they should include their full context, namely the recited bits “of” a PCI bus transaction.

Second, Defendants’ proposed construction reads out of all claims the recitation of specific bits of a PCI bus transaction and limits all claims to an entire PCI bus transaction.<sup>8</sup> When an Asserted Claim recites conveying or transmitting specific bits of a PCI bus transaction, that claim requires only the conveyance or transmission of those specific bits, regardless of those bits’ origin. Under Defendants’ construction, not only must those bits be conveyed/transmitted, but there must also be an entire PCI bus transaction from which those bits are derived.

---

<sup>8</sup> Based on this and Defendants’ other proposed constructions, all claims reciting a “PCI bus transaction” in any manner would require conveying/transmitting an entire PCI bus transaction.

Further, although certain claims separately reference conveying/transmitting “the PCI bus transaction,”<sup>9</sup> in all instances, “the PCI bus transaction” takes its antecedent basis from the limitations reciting specific bits of a PCI bus transaction and thus refers to the same recited bits.<sup>10</sup>

**E. Claims reciting a [Peripheral Component Interconnect] PCI bus transaction, or an encoded [Peripheral Component Interconnect] PCI bus transaction, “in [a] serial form” or “serially encoded” or “in a serial bit stream”**

<b>'797 claims 7, 14, 36; '768 claims 1, 2, 4, 13, 17, 39; '750 claims 1, 2, 5, 7, 10, 12, 21, 31, 34, 35, 44; '654 claim 21, 24, 26, 35; '140 claim 30, 31, 34</b>	
<b>ACQIS's Construction</b>	<b>Defendants' Construction</b>
<p>“Encoding” terms, reciting conveying/transmitting <i>encoded</i> address and data bits of a PCI bus transaction or <i>encoded</i> address bits, data bits, and byte enable information bits, should be given their plain and ordinary meaning, wherein the plain and ordinary meaning of “encoded” is “code representing [the recited bits of] a PCI bus transaction.”</p> <p>“Serial” terms, reciting conveying/transmitting (1) address and data bits of a PCI bus transaction, or (2) address bits, data bits, and byte enable information bits, “in [a] serial form,” or “serially,” or “in a serial bit stream,” should be given their plain and ordinary meaning.</p> <p>The <i>EMC</i> construction of “[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction” and related terms applies only to certain claims and terms, i.e., “claims reciting an ‘encoded’ PCI bus transaction” and more specifically, “terms that recite (1) ‘encoded,’ (2) ‘serial,’ and (3) ‘PCI bus transaction.’” Ex. 41, <i>ASUSTeK</i>, Dkt. 144 at 2.</p>	<p>“a PCI bus transaction that has been serialized from a parallel form”</p>

ACQIS's proposals relating to these terms align with this Court's previous constructions

<sup>9</sup> ACQIS notes for clarity that in Defendants' discussion of claims that “further recite preserving, conveying, or transmitting ‘the PCI bus transaction,’” Defendants identify claims from the Asserted Patents that ACQIS has *not* asserted against either Microsoft or Sony, i.e., '797 claims 1, 4, 10, 18, 21; '768 claims 6, 11, 12, 16, 18-21, 23-25, 28, 29, 31-33, 35, 38; '750 claims 6, 11, 16, 17, 19, 22, 23, 26, 28, 30, 37, 38, 47; '654 claims 14, 17. *See* Defs. Br. at 19.

<sup>10</sup> If, however, in a given claim there is any limitation construed to require a complete PCI bus transaction, that is a separate limitation independent of the limitation reciting conveyance/transmission of specific bits “*of* a PCI bus transaction.”



and applications of the constructions from *EMC* and account for the difference that the *EMC* claims recite conveying a complete PCI bus transaction, and all Asserted Claims here recite conveying specific bits of a PCI bus transaction. The *EMC* construction of “[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction” includes a complete transaction: “a *PCI bus transaction* that has been serialized from a parallel form.” *EMC Claim Construction*, 2017 WL 6211051, at \*8 (emphasis added); *EMC Summary Judgment*, 2021 WL 1088207, at \*5-6. Where a claim requires conveying only specific “encoded” *bits* of a transaction, it does not make sense to apply, without modification, a construction that requires a complete transaction.

Defendants mischaracterize the nature and scope of the parties’ agreement regarding these terms. *See* Defs. Br. at 21. ACQIS acknowledges this Court’s previous decision on “encoded” terms in *ASUSTeK*, including the Court’s conclusion that *EMC* applies to certain claims and terms, i.e., “claims reciting an ‘encoded’ PCI bus transaction” and more specifically, “terms that recite (1) ‘encoded,’ (2) ‘serial,’ and (3) ‘PCI bus transaction.’” Ex. 41, *ASUSTeK*, Dkt. 144 at 2. But ACQIS does not agree that claims that recite conveying specific “encoded” bits of a PCI bus transaction should be construed to require a complete, “encoded” PCI bus transaction.

Much of Defendants’ argument depends on the incorrect assertion “there is no dispute that a PCI bus transaction, when it is generated, is in a parallel form.” Defs. Br. at 22. A PCI bus transaction need not originate in parallel form. Figures 8A and 8B from ’768/’750/’797 (Figures 19 and 20 in ’654/’140), which depict embodiments corresponding to the Asserted Claims here, illustrate a serial LVDS channel direct from a chip with no parallel PCI bus, and therefore no need for any PCI bus transaction (or particular bits of a PCI bus transaction) to originate in parallel form. Claim language that recites conveying or transmitting bits of a PCI bus transaction “in [a] serial form,” “in a serial bit stream,” or “serially” requires only that the bits be

conveyed/transmitted in serial form, not that they first be converted from parallel to serial form.

The specifications of the Asserted Patents describe certain embodiments, upon which Defendants focus, in which parallel PCI bus transactions originating on a parallel PCI bus are converted from parallel to serial form. *See* Defs. Br. at 23-24. The Asserted Claims do not recite these embodiments, however, and do not require parallel to serial conversion (or that recited bits of a PCI bus transaction originate in parallel form).

The *EMC* prosecution disclaimer finding arose from IPRs addressing two patents not at issue here: U.S. Patent Nos. 8,041,873 and RE42,814. *EMC Claim Construction*, 2017 WL 6211051, at \*1, \*5-8. The prosecution disclaimer for the '873 and '814 patents does not apply to the different patents here, which include different claim language and disclosures. *See Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1323 (Fed. Cir. 2013) (finding that prosecution disclaimer did not attach to patent family member based on the family member's intrinsic record).<sup>11</sup> Notably, the '873 and '814 patents for which the *EMC* court found disclaimer do not include Figures 8A and 8B, corresponding to the claims here, which illustrate a serial LVDS channel direct from a chip with no parallel PCI bus. *See* Ex. 10 ('873 patent); Ex. 13 ('814 patent). These different disclosures “directly contradict” the *EMC* prosecution disclaimer finding, and therefore that finding does not attach to the patents asserted here. *Trading Techs.*, 728 F.3d at 1323; Ex. 21, *Samsung*, Dkt. 92 at 26 (finding that disclaimer does not apply to the Asserted Patents); *see also* Ex. 48, *Samsung*, Dkt. 116 at 1 (overruling objections).

This Court previously concluded that the *EMC* constructions apply *only* to claim terms that include a “PCI bus transaction” that is “encoded” *and* conveyed in a “serial” form. Ex. 41,

---

<sup>11</sup> The '654 and '140 patents asserted here do not claim priority to either the '873 or '814 patents, so the *EMC* prosecution disclaimer finding cannot attach. *Trading Techs.*, 728 F.3d at 1323 (explaining that disclaimer can extend to patents in the same lineage).

*ASUSTeK*, Dkt. 144 at 2. This Court considered and rejected the argument, made again by Defendants here, that the *EMC* construction applies to Asserted Claims that do not recite the word “encoded.” Defendants provide no justification for construing all the terms the same whether they include “encoded” or not. Defendants’ proposed construction improperly renders “encoded” meaningless and therefore should not be adopted. *See Wasica Finance*, 853 F.3d at 1288 n.10.

Finally, given the significant differences in claim language, including that the Asserted Claims do not even recite conveying a complete, “encoded” PCI bus transaction, “encoded” as used in the Asserted Claims should be accorded its plain and ordinary meaning, consistent with ACQIS’s proposed construction. *See* Ex. 55, *ASUSTeK*, Dkt. 55 at 8.

**F. “console”**

’750 claims <u>5</u> , 7, <u>10</u> , 12, <u>24</u> , <u>35</u> , <u>44</u> ;’654 claims <u>20</u> , 21, <u>23</u> ; ’140 claims <u>14</u> , 15, 17, <u>18</u> , 19, 21, <u>31</u> , <u>34</u>	
ACQIS’s Construction	Defendants’ Construction
“a chassis or enclosure, housing one or more coupling sites, that connects components of a computer system”	“a chassis that connects several components of a computer system”

This Court has previously construed “console.” Ex. 55, *ASUSTeK*, Dkt. 52 at 10. ACQIS’s proposed construction adopts this Court’s previous construction. Defendants instead seek adoption of an agreed construction of “console” from *Appro* (2010) applied in *Alcatel-Lucent* (2013), neither of which involved any Asserted Patent. *See ACQIS LLC v. Alcatel-Lucent USA Inc.*, No. 6:13-cv-638, 2015 WL 1737853, at \*1, \*7 (E.D. Tex. Apr. 13, 2015). Defendants do not otherwise attempt to support their proposed construction.

The ACQIS specifications support this Court’s previous construction:

The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. *The console is an enclosure that is capable of housing each coupling site.*

Ex. 1, '768 at Abstract (emphasis added); *see also id.* at 4:31-35; 4:46-50. A console thus houses coupling sites comprising connectors, consistent with this Court's previous construction. The specification also provides an example of a console that includes "a chassis and a motherboard," (*id.* at 10:57-11:2), indicating that a console can include a motherboard, and not a mere chassis alone. This Court's prior construction adopts these attributes of a console and does not improperly limit a console to a "chassis," and it should therefore be adopted here.

**G. "USB" / "Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol [data/information]"**

'797 claims <u>33</u> , <u>34</u> ; '768 claim <u>40</u> ; '750 claims <u>7</u> , <u>24</u> ; '654 claims <u>20</u> , <u>21</u> , <u>23</u> ; '140 claims <u>15</u> , <u>18</u> , <u>19</u> , <u>21</u> , <u>34</u> , <u>36</u>	
ACQIS's Construction	Defendants' Construction
No construction necessary. These phrases should be given their plain and ordinary meaning.	"[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard"

This Court previously rejected essentially the same construction Defendants propose here and determined that these terms should be given their plain and ordinary meaning. Ex. 55, *ASUSTeK*, Dkt. 52 at 9. This Court's previous determination should be adopted here.

Like the PCI-related claims, the USB-related claims do not require every aspect of the USB specifications. The claims do not recite a Universal Serial *Bus* and all the aspects of the USB specifications required to implement such a bus. The USB-related claims here recite an LVDS channel for communicating certain USB information in opposite directions, such as "protocol data packets," (Ex. 2, '750 at 43:28-32 (claim 24)), "protocol data," (Ex. 3, '797 at 42:8-15 (claim 33)), and "protocol information," (Ex. 5, '140 at 23:15-20 (claim 18)).

The plain claim language indicates that the claims do not require adherence to all aspects of the USB specification. The ACQIS claims reciting LVDS channels to convey USB "data" refer

to information described in the USB specifications relating to the “data payload.” The USB specifications describe a “data field” to communicate data using a USB protocol. Ex. 57, USB 1.0 at § 8.4.3; Ex. 46, USB 2.0, at § 8.4.4. The USB specifications explain that “[t]he data payload is the data that is carried in the data field of a data packet within a bus transaction (as defined in Chapter 8).” Ex. 57, USB 1.0, at § 5.3.2; Ex. 46, USB 2.0, at § 5.3.2.

The claim term “Universal Serial Bus (USB) protocol information” uses more general language than the terms addressing USB “data,” covering any information described in the USB specifications. The ACQIS specifications describe “data” as a subset of “information” generally. *See, e.g.*, Ex. 1, ’768 at 21:37-22:42 (explaining that Figures 13 and 14 show “information transmitted on the XPBus,” including “data” bits and also including other information).

Defendants’ proposed construction seeks to limit the claims to the USB 2.0 and prior versions. Defendants cite two cases, *Fundamental Innovation Systems* (“*FISI*”) and *Uniloc*, which do not support Defendants’ construction. *FISI* addresses claims that include USB-related limitations, e.g., a USB adapter and a USB connector. *Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co., Ltd.*, No. 2:17-cv-145-JRG-RSP, 2018 WL 647734, at \*6-8 (E.D. Tex. Jan. 31, 2018). The claims in *FISI* add to USB 2.0—they add limitations to USB-compliant features and do not alter the claimed features of the applicable USB standards, e.g., they do not improve or modify the USB connector or adapter. *Id.* at \*7-8.

In contrast, the ACQIS claims reference aspects of USB generally, e.g., “[USB] protocol data,” but with a full-duplex physical interface (i.e., the claimed unidirectional, serial channels that transmit data in opposite directions) that departs from the half-duplex, bidirectional differential signal pair of USB 2.0. *See, e.g.*, Ex. 46, USB 2.0 at 17 (Fig. 4-2) (showing bidirectional D+/D- data wires); Ex. 49, Sarhan Decl., ¶¶ 66-67. Unlike in *FISI*, the ACQIS claims are *not* limited to

USB 2.0 because they explicitly depart from the teachings of USB at the time.

In *Uniloc*, the court found the claims not limited to the Bluetooth specifications that existed at the time of the claimed inventions. *Uniloc USA, Inc. v. Apple, Inc.*, No. 19-cv-1692-EJD (VKD), 2021 WL 432183, at \*8-9 (N.D. Cal. Jan. 15, 2021). The court construed the disputed terms as defined in the Bluetooth specifications that existed at the time of the claimed invention “*and that remain in later versions of the Bluetooth specification.*” *Id.* at \*9 (emphasis added).

Defendants’ proposed construction also seeks to improperly narrow the scope of the “USB” terms to require conveying full USB transactions, i.e., that USB data/information be “conveyed according to the protocols defined in” USB 2.0, regardless of the specific language of each claim. Defendants’ proposed construction improperly limits the claims and renders expressly recited terms superfluous. *See Wasica Finance*, 853 F.3d at 1288 n.10.

#### H. “serial bit channels” and “serial channel”

<b>'797 claims <u>33</u>, 34; '750 claims <u>10</u>, 12; '654 claim <u>20</u>, 21; '140 claims <u>14</u>, 15, <u>17-19</u>, 21, <u>30</u>, <u>31</u>, 34, <u>35</u>, 36, 38</b>	
<b>ACQIS’s Construction</b>	<b>Defendants’ Construction</b>
No construction necessary. These terms should be given their plain and ordinary meaning.	“a path on which units of information are transferred serially from one component to another”

Defendants give no reason why these terms would benefit from construction, and they seek to bind ACQIS to a prior agreed construction regarding different claims and patents. Defendants’ construction provides no clarity: by including “serially,” it does not define “serial.” It also creates a new limitation that the “serial [bit] channel(s)” transfer units of information “from one component to another.” The claims themselves specify where data flows on the claimed “serial [bit] channel(s).” The new term “component” also could introduce ambiguity as to what satisfies that term. Defendants’ construction addresses no dispute and should not be adopted.

Dated: June 9, 2023

Respectfully submitted,

By: /s/ Logan J. Drew

Ronald J. Schutz (admitted in this District)  
MN Bar No. 0130849  
Email: rschutz@robinskaplan.com  
Aaron R. Fahrenkrog (*pro hac vice*)  
MN Bar No. 0386673  
Email: afahrenkrog@robinskaplan.com  
Logan J. Drew (admitted in this District)  
MN Bar No. 0389449  
Email: ldrew@robinskaplan.com  
William Jones (*pro hac vice*)  
MN Bar No. 0402360  
Email: wjones@robinskaplan.com  
**ROBINS KAPLAN LLP**  
2800 LaSalle Plaza  
800 LaSalle Avenue  
Minneapolis, MN 55402  
Telephone: 612-349-8500  
Facsimile: 612-339-4181

Of Counsel:  
T. John Ward, Jr.  
Texas State Bar No. 00794818  
Email: jw@wsfirm.com  
Andrea L. Fair  
Texas State Bar No. 24078488  
Email: andrea@wsfirm.com  
**WARD, SMITH & HILL, PLLC**  
1507 Bill Owens Parkway  
Longview, TX 75604  
(903) 757-6400 (telephone)  
(903) 757-2323 (facsimile)

**CERTIFICATE OF SERVICE**

I hereby certify that on June 9, 2023, I electronically filed the foregoing with the Clerk of Court using the CM/ECF system, which will send notification of such filing via electronic mail to all counsel of record.

/s/ Logan J. Drew  
Logan J. Drew